Candidate’s Declaration

I hereby declare that the work, which is being presented in the Dissertation entitled “DESIGN AND SIMULATION OF 64 BIT ALU WITH 32 OPERATIONS IN VHDL” in partial fulfillment for the award of Degree of “Master of Science” in Department of Physics & Electronics and submitted to the **Department of Physics & Electronics, Faizabad,** Dr. Ram Manohar Lohia Avadh University is a record of my own investigation carried under the Guidance of Prof.K.K. Verma, Department of Physics & Electronics, Faizabad.

I have not submitted the matter presented in this Dissertation anywhere for the award of any other Degree.

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**Supervisor**

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**CERTIFICATE**

This is to certify that this Dissertation entitled “DESIGN AND SIMULATION OF 64 BIT ALU WITH 32 OPERATIONS IN VHDL” has been successfully carried out by Vikash Pandey, under my supervision and guidance, in partial fulfillment of the requirement for the award of **Master of Science** Degree in VLSI design from Department of Physics & Electronics, Faizabad for the year 2017-18.

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**ACKNOWLEDGEMENT**

I wish to express my deep sense of gratitude towards my guide **Prof.(Dr.) K.K. Verma** (Professor and Head, Department of Physics & Electronics**,** Faizabad) for his guidance, many motivating discussions, encouraging support andfor providing me all the necessary facilities which were invaluable for me to the completion of this work.

Words are inadequate in offering my gratitude to my internal review **Mr. Sanjay Jaiswal,** Guest lecturer, Department of Physics & Electronics**,** Faizabad, for his expert and valuable guidance backed with constant encouragement.

I take immense pleasure in thanking all the faculty members, staff members and my colleagues for their valuable assistance in the project work.

I would like to express my special thanks to my friends and all those who helped me directly or indirectly in completion of this dissertation.

Finally, yet important, I would like to express my heartfelt thanks to my beloved parents, my sister, my mother for their help, support in all the circumstances and kept my moral always high.

I render my gratitude to the God who gives self- confidence, ability and strength in me to complete this work for not allow me down at the time of crisis and showing me the silver lining in the dark clouds as well as expressing my apology that I could not mention personally one by one.

Vikash Pandey

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